REMARKS

The enclosed is responsive to the examiner's Final Office Action mailed on July 7, 2009. At the time the examiner mailed the Final Office Action, claims 19-23 were pending. No claims are amended or canceled or added. As such, claims 19-23 are now pending. Applicants respectfully request reconsideration of the present application.

35 U.S.C. 103(a) Rejections

The Office Action rejected claims 19 and 23 under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent 7,100,020 (hereinafter "Brightman") in view of U.S. Patent 5,740,406 (hereinafter "Rosenthal"). Applicants respectfully submit that the combination of Brightman and Rosenthal does not describe what these claims require.

Brightman describes an integrated circuit for use in processing streams of data and packets, including a number of packet processors. (Brightman, Abstract). In particular, Brightman describes a packet processor 303 that includes a header generator 1709 and outputs a fabric frame formed by merging an internally generated header with a payload received from buffer memory 229. (Brightman, col. 34, lines 29-46; col. 35, lines 14-28; Figures 16-18).

Rosenthal describes an input circuit for an input/output device adapted for use in a computer system. (Rosenthal, Abstract).

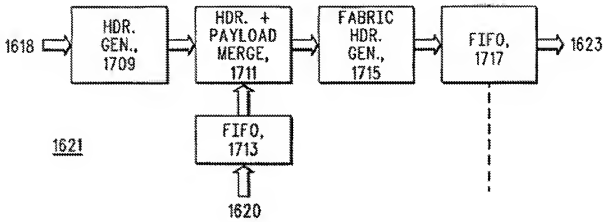
With respect to claim 19, the combination does not describe:

> A device comprising:
> first circuitry to generate a packet based on packet header data received from and generated by a micro-engine and packet payload data from a memory controller, wherein the packet payload data bypasses the micro-engine, the first circuitry comprising

second circuitry to receive the packet payload data from the memory controller, and to store the packet payload data in first-in first-out (FIFO) circuitry; and

third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry.

The combination does not describe "first circuitry to generate a packet based on packet header data received from and generated by a micro-engine..." (Emphasis added). The Office Action alleges that the fabric processor 303 of Brightman describes this circuitry. Specifically, the Office Action asserts that "Tx fabric processor 1605" in the fabric processor 303 meets this limitation. (Office Action, 07/07/09, page 3). Applicants respectfully disagree with the Office Action's interpretation of the cited reference for several reasons. First, there is no "Tx fabric processor 1605." Brightman's 1605 is a MUX as detailed in col.34 l.41. Second, the Tx fabric processor 1621 does not "generate a packet based on packet header data received from and generated by a micro-engine and packet payload data from a memory controller, wherein the packet payload data bypasses the micro-engine." The Tx fabric processor 1621 is illustrated in in Fig. 17 and is discussed in detail below.



This Tx fabric processor 1621 consists of five parts. The first part is "header generator 1709" "which generates frame header 1805 using information that fabric control engine 1601 has placed in merge space 1615." (Brightman, col.35 ll.18-20 and Fig. 17) (emphasis added). This frame header 1805 is passed to "header and payload merge 1711, which merges header 1805 with payload 1807 DMA'ed via path 1620 from buffer memory 229." (Brightman, col.35 ll.20-22 and Fig. 17). FIFO 1713 apparently temporarily stores the payload before it is passed to the header and payload merge 1711. (*See* Brightman, col.35 ll.26-28.) The output of the header and payload merge 1711 is unclear, but it is presumably frame 1801. (*See* Brightman, col.35 ll.22-25.) Next, the fabric header generator 1715 "generates fabric header 1803 and adds it to frame 1801." (Brightman, col.35 ll.22-24.) This frame 1801 then is output to "switch fabric 222" through FIFO 1717 which "permits fabric processor 303 and switch fabric 222 to run at different speeds." (Brightman, col.35 ll.25-26.) As discussed, no component of the Tx fabric processor 1621 "generate[s] a packet based on packet header data received from and generated by a micro-engine..." as the Tx fabric process generates, twice, a header information. Third, there is no support that Brightman describes the use of a micro-engine much less one that generates packet header data or that "packet payload data bypasses the micro-engine." Rosenthal is not cited as being relevant to this limitation and Applicants respectfully agree.

The Office Action correctly recognizes that "Brightman does not specifically show the details of a third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry...." (Office Action, 07/07/09, page 4, emphasis added). However, the Office Action purports that "the above-mentioned claim limitations are well-established in the art as evidenced by Rosenthal..." Applicants respectfully disagree with this assertion. First, the FIFO of Rosenthal stores commands not packet payload data. Second, Rosenthal, like

Brightman, fails to show the details of circuitry to implement the operation of the pointers. Third, the combination does not describe circuitry "to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry." While the pointers of Rosenthal help its system ascertain the free space available, it does not assist in the alignment of anything. This is not a surprise given that Rosenthal has nothing to do with packets or the transmission thereof. Finally, Applicants respectfully submit that one of ordinary skill in the art would not have reason nor be motivated to combine the cited references in the manner purported by the Office Action. As discussed above, Brightman is directed to processing streams of data and packets. Brightman's FIFO 1713, located inside of the Tx fabric processor, is designed to provide the flexibility needed to deal with delays in access memory data, and his FIFO design solves the memory data delay access problem. Rosenthal provides an input/output device, including an internal FIFO, adapted for use in a computer system to process application program commands. Rosenthal's input/output device is an I/O device that connects with its system processor via a memory bridge. As shown, Brightman's FIFO, located inside a processor, is designed to deal with delays in access memory data, while Rosenthal's FIFO, located inside an I/O device under the control of its system processor, is designed to receive application program commands sent from the processor. Moreover, there has been no showing that there would be motivation to add the pointer functionality to Brightman's FIFO which apparently works just fine without it.

Accordingly, the combination of Brightman and Rosenthal does not describe what Applicants claim 19 requires. Claims 20-22 are dependent on claim 19 and are allowable for at least the same rationale.

With respect to claim 23, the combination of Brightman and Rosenthal fails to describe the limitations for reasons similar to those stated with respect to claim 19.

The Office Action rejected claim 20 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 7,100,020 (hereinafter "Brightman") in view of U.S. Patent 5,740,406 (hereinafter "Rosenthal") in further view of U.S. Patent 6,829,240 (hereinafter "Lincoln"). Claim 20 is dependent on claim 19 and allowable for at least the same rationale.

The Office Action rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 7,100,020 (hereinafter "Brightman") in view of U.S. Patent 5,740,406 (hereinafter "Rosenthal") in further view of U.S. Patent 6,061,361 (hereinafter "An"). Claim 21 is dependent on claim 19 and allowable for at least the same rationale.

The Office Action rejected claim 22 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 7,100,020 (hereinafter "Brightman") in view of U.S. Patent 5,740,406 (hereinafter "Rosenthal") in further view of U.S. Patent 5,878,217 (hereinafter "Cherukuri"). Claim 22 is dependent on claim 19 and allowable for at least the same rationale.

CONCLUSION

Applicants respectfully submit that all rejections have been overcome and that all pending claims are in condition for allowance.

If there are any additional charges, please charge them to our Deposit Account Number 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact David F. Nicholson at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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/David F. Nicholson/

David F. Nicholson
Reg. No.: 62,888

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300